define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

The various embodiments of the present invention are directed to a semiconductor package assembly having a plurality of relatively thin strips of a compliant adhesive film to adhere a semiconductor die to a substrate or interposer. The compliant adhesive film is interposed between the semiconductor die and the interposer and is generally segmented into a plurality of elongated strips having narrow widths. The compliant adhesive film thus reduces failures in semiconductor package interconnections, such as solder bonds, by reducing undesired shear stresses that may result from unmatched coefficients of thermal expansion for the interposer and the semiconductor die. A further advantage associated with the various embodiments of the invention is that the cumulative thermal expansion for multiple, relatively narrow strips of adhesive film is less than the thermal expansion for one or more relatively wide layers of an elastomeric film. As a consequence, the stress on the package wire bond joints resulting from the different coefficients of thermal expansion between the die and the substrate are reduced. The use of the relatively narrow strips of the compliant adhesive film has significant advantages over one or more relatively wide strips of material, as discussed more fully in the application at pages 8 through 9 of the application.

The Examiner has cited the Mitchell reference as pertinent to the patentability of claims in the present case. Mitchell discloses a semiconductor chip package. The package includes a semiconductor chip and a printed wire board (PWB) spaced apart from the semiconductor chip. Positioned between the chip and the PWB is a plurality of elastic compliant pads forming columnar supports for the chip. Referring first to Figure 1, the elastic compliant pads 110 are clearly shown. The compliant pads 110 are made of a curable liquid elastomer, such a silicone elastomer (col. 5, lines 2-6). The pads are arranged in a grid pattern (col. 5, lines 15-18) using a stencil mask (col. 5, lines 25-30). The Examiner has further referred to Figure 4B of Mitchell as depicting an elongated adhesive pad 110 positioned between the semiconductor chip and the PWB. However, the applicant notes that the pad 110 is comprised of the curable liquid elastomer referred to earlier, and fails to disclose elongated strips of a compliant adhesive film, the strips including a compliant carrier layer and having a pair of opposing surfaces having adhesive layers disposed on the surfaces.

The Examiner has also cited the Chan reference. Chan discloses a semiconductor package having a multi-layered lead frame assembly. With reference to Figure 1 of Chan, a package 10 is shown having a pair of dual-sided adhesive tape strips 20 that extend substantially the length of a semiconductor circuit chip 12. The adhesive tape strips 20 further extend *substantially across* a width of the semiconductor circuit chip 12 so that a main lead frame 22 may be positioned and supported on a side of the adhesive tape strips 20 that opposes the side applied to the semiconductor circuit chip 12. A narrow gap is defined between the pair of adhesive tape strips 20 to permit the lead frame 22 to be electrically bonded to a plurality of bond pads 18 that are arranged along a bisecting axis 14 of the semiconductor circuit chip 12.

In a further embodiment, as best seen in Figure 3 of the Chan reference, similar wide adhesive tape strips 20 are used to mount a preformed lead frame structure 22 onto a surface of the semiconductor circuit chip 12. Again, applicant notes that the adhesive tape strips 20 possess a combined width that is substantially the entire width of the semiconductor circuit chip 12, and that a narrow separation is defined between the respective strips 20 only to permit the lead frame structure 22 to be electrically coupled to the plurality of bond pads 18 that are positioned along a central bisecting axis 14.

Applicant therefore understands the Chan reference to disclose relatively wide adhesive strips 20. The relatively wide adhesive strips are required since the lead frame extends substantially across the width of the semiconductor chip, and must be securely anchored to the underlying chip. In addition, since the adhesive strip forms an electrically insulative layer, the strips must necessarily be wide so that adequate electrical isolation is achieved between the chip surface and the superimposed lead frame. The applicant finds no reference to narrow strips of adhesive material as disclosed in the present application, and further finds *absolutely no reference* in Chan to the thermal mismatch difficulties discussed in detail in the present application, much less *any reference* that suggests that the package disclosed by Chan may be used to reduce thermal mismatch problems in semiconductor packages. If the undersigned has missed a relevant teaching in the Chan reference that is pertinent, the Examiner is requested to contact the undersigned attorney to particularly point out where this pertinent reference may be found.

Turning now to the claims, differences between the specific claim language and the applied art will be pointed out. Claim 1 recites in pertinent part, " A semiconductor device

package, comprising...a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of opposed lateral edges...at least one electrically conductive external terminal...an interposer having a die attach surface and an external surface opposite of the die attach surface disposed in between the semiconductor die and the at least one external terminal, the interposer having at least one electrically conductive interconnect electrically coupling the at least one bond pad of the semiconductor die positioned adjacent to the die attach surface to the at least external terminal positioned adjacent to the external surface, the interposer being formed of an organic substrate or a polyimide substrate; and *a plurality of elongated strips of compliant adhesive film,* each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges and disposed between the semiconductor die and the interposer, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges of the semiconductor die...*" (Emphasis added). The Mitchell reference does not disclose this. Instead, Mitchell discloses columnar structures comprised of a uniformly elastomeric material. Chan does not disclose narrow strips of adhesive film where a sum of the widths of the strips is substantially less than the width of the die. Instead, Chan discloses wide strips extending substantially the entire width of the die to affix a leadframe to the die and to provide sufficient insulation of the leadframe from the die. Accordingly, claim 1 is allowable over the cited art. Further, claims depending from claim 1 are also allowable based on the allowability of the base claim and further in view of the additional limitations recited therein.

Claim 11, as amended recites in pertinent part, "A device package assembly for a semiconductor die being constructed from a process comprising...laminating a plurality of strips of compliant adhesive film to an interposer having at least one electrically conductive interconnect, the interposer being formed of an organic substrate or a polyimide substrate and further having a die attach surface to which the semiconductor die is attached, and an external surface opposite of the die attach surface...attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges, the strips of compliant adhesive film having a first length and a second length perpendicular to the first length, the first

length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips further including a compliant carrier layer* ..." (Emphasis added). Again the Mitchell reference does not disclose adhesive strips having a compliant cover layer. Chan further does not disclose that the adhesive strips are substantially narrow strips. Instead, the strips extend *in width* substantially across the entire die to hold a leadframe in place on the die and to insulate the leadframe from the die surface. Therefore, claim 11 is allowable over the cited art. Further, claims depending from claim 11 are also allowable based on the allowability of the base claim and further in view of the additional limitations recited therein.

Claim 38 as amended recites in pertinent part, "A semiconductor device package, comprising...a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges...an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate...and...*a plurality of elongated strips of compliant adhesive film,* each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges...*". (Emphasis added). As pointed out in grater detail above, Mitchelll does not disclose strips of compliant film. Instead, Mitchell discloses columnar supports of an elasstomeric material. Although Chan discloses the adhesive strips, the disclosed strips are wide strips suited for affixing a leadframe assembly to a die that provides the required insulation between the die and the leadframe. Chan does not disclose the relatively narrow strips that are required to accommodate a thermal mismatch between an interposer and a die. Accordingly, claim 38 is allowable over the cited art. Further, claims depending from claim 38 are also allowable based on the allowability of the base claim and further in view of the additional limitations recited therein.

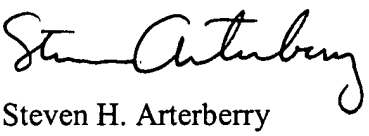
Finally, claim 42, as amended recites in pertinent part, "A semiconductor device package, comprising...a semiconductor die having a first surface on which at least one electrically conductive bond pad is fabricated, the die having first and second pairs of lateral edges...an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate...and...*a plurality of elongated strips of compliant adhesive film*, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die to adhere the semiconductor die to the die attach surface of the interposer, *a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips of compliant adhesive film further including a compliant carrier layer...*" (Emphasis added). Again, Mitchell and Chan do not singly, or in any motivated combination, disclose this. Accordingly, claim 42 is allowable over the cited art. Further, claims depending from claim 42 are also allowable based on the allowability of the base claim and further in view of the additional limitations recited therein.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made**".

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Steven H. Arterberry
Registration No. 46,314

SHA:sj

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)

1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Four Times Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of opposed lateral edges;

at least one electrically conductive external terminal;

an interposer having a die attach surface and an external surface opposite of the die attach surface disposed in between the semiconductor die and the at least one external terminal, the interposer having at least one electrically conductive interconnect electrically coupling the at least one bond pad of the semiconductor die positioned adjacent to the die attach surface to the at least external terminal positioned adjacent to the external surface, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges and disposed between the semiconductor die and the interposer, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges of te semiconductor die, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.

11. (Four Times Amended) A device package assembly for a semiconductor die being constructed from a process comprising:

laminating a plurality of strips of compliant adhesive film to an interposer having at least one electrically conductive interconnect, the interposer being formed of an organic substrate or a polyimide substrate and further having a die attach surface to which the semiconductor die is attached, and an external surface opposite of the die attach surface;

attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges, the strips of compliant adhesive film having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die; and

bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad.

38. (Three Times Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of

the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.

42. (Four Times Amended) A semiconductor device package, comprising:

a semiconductor die having a first surface on which at least one electrically conductive bond pad is fabricated, the die having first and second pairs of lateral edges;

an interposer having a die attach surface and at least one electrically conductive interconnect electrically coupled to at least one bond pad of the semiconductor die, the interposer being formed of an organic substrate or a polyimide substrate; and

a plurality of elongated strips of compliant adhesive film, each strip having a first length and a second length perpendicular to the first length, the first length being substantially greater than the second length, the strips extending substantially the entire distance between the first pair of opposed lateral edges between the die attach surface and the semiconductor die to adhere the semiconductor die to the die attach surface of the interposer, a sum of the second lengths of the elongated strips being substantially less than a distance between the second pair of opposed lateral edges, the strips of compliant adhesive film further including a compliant carrier layer having a pair of opposing surfaces with a first adhesive layer disposed on a first surface of the opposing surfaces of the carrier layer to adhere the semiconductor die to the die attach surface of the interposer, and a second adhesive layer disposed on a second surface of the opposing surfaces of the carrier layer to adhere the carrier layer to the die.